

REMARKS

This Amendment is being preliminarily submitted for the purpose of effecting minor editorial/grammatical revisions with regard to original claim 1 of this application as well as in consideration of submitting an additional set of claims to further define the invention including in terms of more fully covering various featured aspects directed thereto, based on the originally submitted disclosure. In that regard, examples of featured aspects covered by the now pending claims 1-9 are illustrated in connection with the example embodiment shown in Fig. 49 of the drawings, although not limited thereto.

Referring to the related example embodiment in Fig. 49, the "first region" of the invention relates to the memory cell portion of Fig. 49, which contains the "first MISFETs" such as Qt and has formed thereover the word and bit lines and the storage capacitor (e.g., C). The "second region" according to the present invention relates to the region in Fig. 49 containing the peripheral circuit transistors such as n-channel MISFETs Qn and P-channel MISFETs Qp. Regarding the "wiring layer" of the present invention, an example thereof can be seen with regard to wiring layer 33A, 33B over the "second region" of the semiconductor integrated circuit device. The plugs, according to claims 1+ and 4+ provide the inter layer electrical connections between the active region of the respective MISFETs. It is submitted, such a scheme as that not covered by claims 1-9 is a clear and patentable improvement over that previously known. Accordingly, examination as well as favorable action therefor of this application is respectfully requested.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (referencing case no. 501.35152CC3).

Respectfully submitted,



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